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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,608	12/24/2003	CHIH-FENG SUNG	10217-US-PA	1607

31561 7590 06/09/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
TRAN, THUY V	
ART UNIT	**PAPER NUMBER**
2821	

DATE MAILED: 06/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	10/707,608	SUNG, CHIH-FENG	
	Examiner	Art Unit	
	Thuy V. Tran	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed 03/24/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a reply to the Applicant's amendment and response submitted on 03/24/2006. In virtue of this amendment and response, claims 1-22 remain pending in the instant application.

Priority Application Translation requested

1. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country. In this case, the prior application is Taiwan 91137270 filed 12/25/2002. However, to assure the foreign priority filing date and the satisfaction of the enablement and description requirements of 35 USC 112, first paragraph, in addition to a certified copy of the foreign application, an English language translation is requested. See MPEP, Sections 201.13 & 706.02(b); 37 CFR 1.55.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.*

3. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Asano et al. (Pub. No.: US 2002/0190924 A1).

With respect to claim 1, Asano et al. discloses, in Fig. 1, an organic light-emitting display (see paragraph [0002], lines 4-5) having a plurality of pixels (PIXEL (i,i)) and a plurality of external power lines [14, 15] (which are common power line and common ground line,

respectively; see paragraph [0026], lines 1-5); the organic light-emitting display being characterized in that each of the external power lines [14, 15] diverts into a plurality of internal power lines (for instance, common power line [14] diverts into a plurality of internal power lines connected to EL_{ii}; see Fig. 1), and each internal power line is electrically connected to at least two of the pixels (see Fig. 1), wherein the internal power lines connected to different external power lines [14, 15] are separated (for instance, common power line [14] having internal power lines connected to Elii while common ground lines having internal power lines connected to one terminal of capacitor Cii and to one terminal of driving transistor Triib; see Fig. 1).

With respect to claim 2, Asano et al. discloses, in Fig. 1, that the external power lines are coupled to a power source [Vo (for common power line [14]) or ground voltage source (for common ground line [15]).

With respect to claim 3, Asano et al. discloses, in Fig. 1, that the power source (for instance, [Vo]) supplies an electric current, and the electric current flows through the internal power lines to reach the pixels.

With respect to claim 4, Asano et al. discloses, in Fig. 1, that the pixels are arranged in a pixel array (having [ixi] matrix).

With respect to claim 5, Asano et al. discloses, in Fig. 1, that each of the pixels comprises (i) a switching transistor [TRiia] having a first drain electrode, a first gate electrode, and a first source electrode, wherein the first drain electrode is coupled to a data line [Yi], and the first gate electrode is coupled to a scan line [Xi], (ii) a driving transistor [TRiib] having a second drain electrode, a second gate electrode, and a second source electrode, wherein the second gate electrode is coupled to the first source electrode, and the second source electrode is grounded

(connected to the common ground line [15]; see Fig. 1), (iii) a storage capacitor [Cii], having a first terminal and a second terminal, wherein the first terminal is coupled to the first source electrode and the second gate electrode, and the second terminal is grounded (connected to the common ground line [15]; see Fig. 1) and coupled to the second source electrode, and (iv) a light-emitting device [ELii], having an anode and a cathode, wherein the anode is coupled to one of the internal power lines (see Fig. 1) and the cathode is coupled to the second drain electrode.

With respect to claim 6, Asano et al. discloses, in Fig. 1, that one terminal of each of the internal power lines is coupled via the external power line to a positive power source (which is the common power source [Vo]).

With respect to claim 7, Asano et al. discloses, in Fig. 1, that the switching transistor [TRiia] comprises a thin film transistor (see paragraph [0030], lines 1-2).

With respect to claim 8, Asano et al. discloses, in Fig. 1, that the driving transistor [TRiib] comprises a thin film transistor (see paragraph [0030], lines 1-2).

With respect to claim 9, Asano et al. discloses, in Fig. 1, that the light-emitting device comprises an organic light-emitting diode [ELii] (see paragraph [0026], line 1).

With respect to claim 10, Asano et al. discloses, in Fig. 2, that the light-emitting device [Elii] comprises a polymer light-emitting diode (since it contains a transparent conductive layer, at least, which is inherently made of polymer (transparent layer)).

With respect to claim 11, Asano et al. discloses, in Fig. 1, that the organic light-emitting device comprises an active matrix organic light emitting display (see paragraph [0002], lines 4-5).

With respect to claim 12, Asano et al. discloses, in Fig. 1, an organic light-emitting display comprising (1) a pixel array [ixi+2] having a plurality of data lines [Y(i), Y(i+1), Y(i+2)]], a plurality of scan lines [X(i), X(i+1), X(i+2)], and a plurality of first and second pixels (whether pixels in row as the first and in column as the second, or vice-versa; see Fig.1), wherein each of the first and second pixels is electrically connected to one of the scan lines and one of the data lines correspondingly (see pixel [11] with connections to the scan line X(i) and the data line [Y(i)]), (2) a first external power line [14], dividing into a plurality of first internal power lines (connected to Elii; see Fig. 1), wherein each first internal power line is electrically connected to at least two of the first pixels (see Fig. 1), (3) a second external power line [15], dividing into a plurality of second internal power lines, wherein each second internal power line is electrically connected to at least two of the second pixels, and the first internal power lines and the second internal power lines are separated, and (4) a power source [Vo] electrically connected to the first and second external power lines (see Fig. 1).

With respect to claim 13, Asano et al. discloses, in Fig. 1, that each of the first and second pixels comprises (i) a switching transistor [TRiia] having a first drain electrode, a first gate electrode, and a first source electrode, wherein the first drain electrode is coupled to one of the data lines [Yi, Y(i+1), Y(i+2)], and the first gate electrode is coupled to one of the scan lines [Xi, X(i+1), X(i+2)], (ii) a driving transistor [TRiib] having a second drain electrode, a second gate electrode, and a second source electrode, wherein the second gate electrode is coupled to the first source electrode, and the second source electrode is grounded (connected to the common ground line [15]; see Fig. 1), (iii) a storage capacitor [Cii], having a first terminal and a second terminal, wherein the first terminal is coupled to the first source electrode and the second gate

electrode, and the second terminal is grounded (connected to the common ground line [15]; see Fig. 1) and coupled to the second source electrode, and (iv) a light-emitting device [ELii], having an anode and a cathode, wherein the anode is coupled to one of the first and second internal power lines (see Fig. 1) and the cathode is coupled to the second drain electrode.

With respect to claim 14, Asano et al. discloses, in Fig. 1, that the switching transistor [TRiia] comprises a thin film transistor (see paragraph [0030], lines 1-2).

With respect to claim 15, Asano et al. discloses, in Fig. 1, that the driving transistor [TRiib] comprises a thin film transistor (see paragraph [0030], lines 1-2).

With respect to claim 16, Asano et al. discloses, in Fig. 1, that the light-emitting device comprises an organic light-emitting diode [ELii] (see paragraph [0026], line 1).

With respect to claim 17, Asano et al. discloses, in Fig. 2, that the light-emitting device [Elii] comprises a polymer light-emitting diode (since it contains a transparent conductive layer, at least, which is inherently made of polymer (transparent layer)).

With respect to claim 18, Asano et al. discloses, in Fig. 1, an organic light-emitting display having a plurality of pixels [PIXEL(i, i)] in a matrix of columns and rows and a plurality of external power lines [14, 15], the organic light-emitting display being characterized in that (1) each of the external power lines diverts into a plurality of internal power lines (connections to elements within the pixels; see Fig. 1), and the pixels in the same column or in the same row are separated into a plurality of groups and the pixels in each group are electrically connected to one of the internal power lines, wherein the internal power lines are electrically connected to the pixels in different groups are separated (see Fig. 1 and the details expressly recited above).

With respect to claim 19, Asano et al. discloses, in Fig. 1, that the external power lines are coupled to a power source [Vo or ground voltage source of [15]].

With respect to claim 20, Asano et al. discloses, in Fig. 1, that the power source supplies an electric current, and the electric current flows through the internal power lines to reach the pixels.

With respect to claim 21, Asano et al. discloses, in Fig. 1, an organic light-emitting display comprising (1) a pixel array having a plurality of data lines [Y(i), Y(i+1), Y(i+2)], a plurality of scan lines [X(i), X(i+1), X(i+2)] and a plurality of first and second pixels arranged in a matrix of columns and rows (see Fig. 1), wherein each of the first and second pixels is electrically connected to one of the scan lines and one of the data lines correspondingly, (2) a first external power line [14], dividing into a plurality of first internal power lines (connections to it within the pixels; see Fig. 1), wherein each first internal power lines is electrically connected to the first pixels in the same column or in the same row, (3) a second external power line [15], dividing into a plurality of second internal power lines (connections to it within the pixels; see Fig. 1), wherein each second internal power lines is electrically connected to the second pixels in the same column or in the same row, wherein the first internal power lines and the second internal power lines are separated (see Fig. 1), and (4) a power source [Vo or ground voltage source of [15]] electrically connected to the first and second external power lines [14, 15].

With respect to claim 22, Asano et al. discloses, in Fig. 1, that that each of the first and second pixels comprises (i) a switching transistor [TRiia] having a first drain electrode, a first gate electrode, and a first source electrode, wherein the first drain electrode is coupled to one of the data lines [Yi, Y(i+1), Y(i+2)], and the first gate electrode is coupled to one of the scan lines

[Xi, X(i+1), X(i+2)], (ii) a driving transistor [TRiib] having a second drain electrode, a second gate electrode, and a second source electrode, wherein the second gate electrode is coupled to the first source electrode, and the second source electrode is grounded (connected to the common ground line [15]; see Fig. 1), (iii) a storage capacitor [Cii], having a first terminal and a second terminal, wherein the first terminal is coupled to the first source electrode and the second gate electrode, and the second terminal is grounded (connected to the common ground line [15]; see Fig. 1) and coupled to the second source electrode, and (iv) a light-emitting device [ELii], having an anode and a cathode, wherein the anode is coupled to one of the first and second internal power lines (see Fig. 1) and the cathode is coupled to the second drain electrode.

Remarks and conclusion

4. Applicant's arguments, see pages 8-14 of the Amendment, filed March 24, 2006, with respect to the rejections of claims 1-22 under 35 U.S.C. 102(b) as being anticipated by Troutman have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, a new ground of rejection is made in view of prior art of record to Asano et al. (Pub. No.: US 2002/0190924 A1). See "Claim Rejections - 35 U.S.C. 102" set forth above for details.

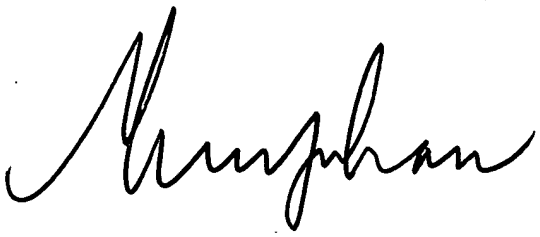
Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuy V. Tran whose telephone number is (571) 272-1828. The examiner can normally be reached on M-F (8:00 AM -4:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

06/07/2006



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PRIMARY EXAMINER